Indonesian Journal of Electrical Engineering and Computer Science
Vol. 17, No. 1, January 2020, pp. 47~60
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v17.i1.pp47-60

Voltage disturbance mitigation in Iraq's low voltage distribution system

Jamal Abdul-Kareem Mohammed[1], Arkan Ahmed Hussein[2], Sahar R. Al-Sakini[3]
[1,3]Electromechanical Engineering Department, University of Technology, Iraq
[2]Electrical Engineering Department, Tikrit University, Iraq

Article Info

Article history:

Received Feb 20, 2019
Revised May 30, 2019
Accepted Jul 31, 2019

Keywords:

DQ0
DVR
Mitigation
Power distribution system
Voltage disturbance

ABSTRACT

Power distribution network in Iraq still suffers from significant problems regarding electricity distribution level. The most important problem is the disturbances that are occurring on lines voltages, which in turn, will negatively affect sensitive loads they feed on. Protection of these loads could be achieved efficiently and economically using the dynamic voltage restorer DVR when installed between the voltage source and load to inject required compensation voltage to the network during the disturbances period. The DVR mitigates these disturbances via restoring the load voltage to a pre-fault value within a few milliseconds. To control the DVR work, dq0 transformation concept and PID method with sinusoidal pulse-width modulation SPWM based converter had been used to correct the disturbances and thus enhance the power quality of the distribution network. The DVR performance was tested by MATLAB/Simulink with all kinds of expected voltage disturbances and results investigated the effectiveness of the proposed method.

Corresponding Author:

Jamal Abdul-Kareem Mohammed,
Department of Electromechanical Engineering,
University of Technology, Baghdad, Iraq.
Email: 50128@uotechnology.edu.iq

1. INTRODUCTION

Nowadays, numerous industries employing advanced technologies for manufacturing and process unit require power supplies with high reliability and high quality. Power quality PQ is described as the variation of voltage, current, and frequency in a power system. Power distribution system should supply their customers with a continuous power flow with a smooth sinusoidal voltage waveform at the amplitude and frequency that has been contracted. The industries like semiconductors, computers, programmable logic controllers, variable speed drives and equipment of manufacturing unit and other nonlinear loads are extremely sensitive to fluctuations that happen on the power supply quality [1], and practically cause various PQ problems [2, 3]. One of the most important prevalent PQ problems is voltage disturbances [4].

The voltage disturbance might come balanced (symmetrical) or unbalanced (asymmetrical) [5]. In balance disturbance, the voltage decreases or increases in all three phases of the power system, simultaneously, while in unbalance case, the voltage decreases and increases in one phase or two phases at the same time. The voltage unbalance disturbance also could be clarified as a case of a poly-phase system when the rms fundamental components of the line voltages and/or the phase angles between successive line voltages, not all are equal. The unbalance voltage disturbances are considered as the major and most common PQ problems in electrical distribution power systems [4]. These disturbances have always existed in power distribution networks due to several reasons like the power system unbalanced faults, irregular distribution of single-phase loads over the three phases, asymmetry of lines, single-phase distributed resources, etc. [1]. Voltage unbalance [6] is the main concern for commercial and industrial electricity consumers because of the

tremendous loss concerning money and time. When analyzing the power system under fault cases, it is necessary to make a distinction between fault types to guarantee the best possible results of the analysis. There are different types of unbalance voltage disturbances may occur on the supply system with the possibility of voltage changes below and above the estimated value. Voltage sag/swell disturbance is often one type of PQ problems, represented by a noticeable voltage drop/rise for a short period (during 50 cycles). Usually, the voltage sag/swell extended for more 50 cycles is known as undervoltage/overvoltage [5].

Generally, the voltage unbalance disturbance are categorized into under-voltage unbalance UVU and overvoltage unbalance OVU [5]. The UVU disturbance is happening as the three-phase voltages have different magnitudes, as well as the positive sequence component is less than the nominal value, whereas the OVU disturbance is occurring when the three-phase voltages are different in magnitude and the value of positive sequence component is higher than the rated value. Switching off a large inductive load or energizing a large capacitor bank is a typical system event that causes the OVU. The OVU is not as important as the UVU, because it is less common in distribution power systems. Notwithstanding, the OVU frequently occurs in many countries at off-peak hours, especially in Iraq circumstances suffering from major problems concerning the fluctuation of electricity distribution voltage levels [7].

Unbalanced voltage disturbances might lead to failing sensitive equipment, or shut down, in addition, to produce unbalance of a large current which may blow fuses or trip breakers. These defects may cause a very high cost to the customer, starting from simple qualitative changes to equipment damage and downtime of production.

Many researchers had been suggested, in the past, various techniques to mitigate the voltage unbalance in power distribution systems such as distribution line reconfiguration [8], phase rearrangement and phase balancing between specific medium voltage feeder and the power distribution energy converter banks with a distribution system [9]. These techniques mostly focus on low and medium voltage side distribution systems. Nevertheless, the proposed solutions did not provide a specific outcome for the effective quality of voltage variation enhancement expected by the customers. Hence, it is not enough to obtain the acceptable standard voltage range of ±5 % [10] of the nominal voltage value at the end-user side. Therefore, there is an urgent need to support secondary distribution systems with modern techniques to ensure a better, effective, cheap and dynamically fast response for mitigation of voltage variation and fluctuation occurring in these systems to complement the existing techniques.

In recent day, the use of manual and automated feeder switching controls is coupled with the many procedures or algorithms to solve the reconfiguration problems [11-13]. Since this is achieved in discrete ways, it cannot purposefully balance the system load; hence, voltage variation correction is not properly achieved. Consequently, the use of advanced solid-state power electronic tools such as uninterrupted power supplies regulators (UPS) [14], super-magnetic energy storage (SMEs) active and passive power filters [15], static var compensator (SVC) [16], distribution series capacitors [17], distribution static compensators (DSTATCOM) [18], unified power quality conditioners (UPQC) [19], etc. can give some voltage variation and voltage fluctuation correction and avoid causing additional unbalanced voltage.

The major drawbacks of UPS, SMEs, DSTATCOM, UPQC, SVCs are basically going back to the difficulty in maintenance, the high cost of facilities, and large size. Hence, it is necessary to employ another custom power device for solving all the previously mentioned problems. In this paper, the dynamic voltage restorer DVR [20-22] is proposed as a successful sort of custom power unit. It has the fastest dynamic response and simplest, more flexible and more cost-effective solution, compared to the other devices [23, 24], to mitigate the voltage disturbances in the secondary distribution system and improve the power quality supplied for electrical loads. This mitigation is accomplished via injection of compensation voltages across the power distribution lines. Therefore, the DVR could be considered as a device that delivers voltages to desired levels and characteristics to facilitate the successful use of sensitive loads.

Disturbance of voltage at the power source side affects the sensitive load performance. Therefore, the DVR is serially connected to the primary distribution lines, at both low and medium voltage levels, between the grid and sensitive loads [25] to protect loads, at most, from voltage disturbances. The DVR can also inject an active/reactive power to the power grids. Besides mitigation of voltage unbalance disturbance [26, 27], the DVR might also add other features like compensation of voltage swells and sags [28, 29], compensation of harmonics [30], power factor correction [31], limiting of fault current [32] and reduction of voltage transients [33].

The DVR proposed in this paper mainly includes three single-phase voltage source inverter VSI units, designed on the basis of the voltage required on the low voltage distribution lines. Each unit has been connected to the distribution system via an injection transformer. In general, the DVR performance is depending upon the control strategy utilized [34]. In this paper, the theory of Synchronous Reference Frame SRF (or dq0) combined with Proportional Integral PI controller and feed-forward open loop voltage control method is employed to compensate for the voltage disturbance. This paper investigates the DVR performance

using MATLAB/Simulink to mitigate the most important PQ problems expected to occur in the low voltage distribution networks in Iraq country, related to the under/over, unbalanced/balanced voltage.

2. DEFINITIONS OF VOLTAGE UNBALANCE

The voltage unbalance can be considered as a disturbance of positive sequence voltage resulting from zero and negative sequence voltage. Thus, it is possible to say that voltage unbalance is a superposition of a negative sequence voltage over a positive sequence voltage. The result of superposition determines the condition whether it is over or under voltage. If the magnitude of a positive sequence component of voltage disturbed is less than (1.0 p.u.), this is called Undervoltage, whereas, for more than (1.0 p.u.), the condition is overvoltage [35].

There are two general definitions [36] for measuring the unbalance voltage given by the international standards NEMA and IEC.

2.1. Definition of NEMA or IEEE

The voltage unbalance percentage (VUP) at machine terminals is defined, by the National Electrical Manufacturer Association Motor and Generator Standard (NEMA MGI), as:

$$VUP\ (\%) = \frac{Max.\ voltage\ deviation\ from\ average\ voltage}{average\ voltage} \times 100\% = \frac{Max.\ (|V_{ab}-V_{avg}|,\ |V_{bc}-V_{avg}|,\ |V_{ca}-V_{avg}|)}{V_{avg}} \times 100\% \quad (1)$$

where $V_{avg} = (V_{ab} + V_{bc} + V_{ca}) / 3$ and V_{ab}, V_{bc} and V_{ca} are the line voltages.

2.2. Definition of IEC or Symmetrical Components

The voltage unbalance factor (VUF) might be specified by the International Electro-technical Commission (IEC) as the voltage ratio of negative sequence component V_n to the positive sequence component V_p.

$$VUF\ (\%) = \frac{|V_n|}{|V_p|} \times 100\% \quad (2)$$

These components are obtained by symmetrical component transformation as follows:

$$V_n = \frac{V_{ab} + a^2 V_{bc} + a V_{ca}}{3} \quad (3)$$

$$V_p = \frac{V_{ab} + a V_{bc} + a^2 V_{ca}}{3} \quad (4)$$

Maintaining the voltage within the statutory limits (±5% voltage) at the end user's terminal is a major challenge for distribution companies [10].

3. DVR SYSTEM CONFIGURATION

A DVR is a custom solid-state custom power device, serially connected near the sensitive load for the purpose of injection of a controlled voltage (compensated voltage) to the electrical distribution network via three single-phase boosting (injection) transformers in order to mitigating the voltage disturbance presented at the point of common coupling, maintaining the load voltage at a desired magnitude and phase and protecting the load from voltage disturbances coming from the network. The main objectives of the DVR are to raise the power capacity utilization of voltage distribution feeders, decrease the power losses and enhance the PQ at the load. The prime hypothesis is neglecting the variations happening on the source voltages. This basically means that the voltage source dynamics are much slower than the load dynamics.

The DVR unit is basically built with three single-phase VSI units, in addition to DC supply or DC charging circuits, harmonic filter circuits, three single-phase injection transformers, and controller. Instead of DC charging circuit, a supercapacitor might be invested to increase the energy storage capacity [37].

The operation of the VSI unit is depending upon the control signals coming from the controlling unit. The DVR is represented by an ideal voltage source. The reference voltage signals are produced from a control algorithm commanded by the control circuit [38]. The DVR is designed according to the voltage

needed on the secondary side of the injection transformer. This transformer provides isolation to the power converter.

Each phase of the proposed topology could be supplied with RLC filters. These filters may be installed on either the primary or secondary side of the transformer. The harmonics appearing across the primary side of the transformer can be removed using RLC filters installed on the inverters' outputs. Usually, the injected voltage magnitudes are separately controlled via three single-phase DVRs. Figure 1 shows the schematic diagram of the DVR.

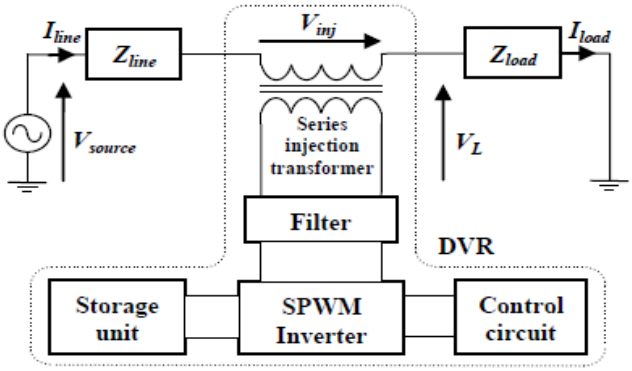

Figure 1. Schematic diagram of the DVR

When a fault happens on low voltage distribution lines, the DVR injects series phase voltage V_{inj} to compensate the load voltage and restore its pre-fault voltage value. The three temporary injected voltage amplitudes should be controlled in order to cancel any harmful effects of a line fault on the load voltage V_{load}. In other word, any differential voltages resulting from disturbances occurring on the voltage distribution lines should be offset by equivalent voltages produced by the inverter and injected to these lines across the booster transformers.

The DVR is autonomously working regardless of the type of fault or any event that may occur in the power system, as long as the entire system keeps linked to the supply grid, which means the line breaker will not trip. In most practical situations, compensation of the negative and positive sequence components of the voltage disturbance noticed at the DVR output could achieve a more economical design. This is very convenient, in the case of the configuration of typical voltage distribution lines, since the zero sequence component of the voltage disturbance will be canceled across the transformer due to its infinite impedance at that component.

The DVR device operates in two modes; standby and boost. In the standby mode of operation (V_{inj}=0), no switching of semiconductors happens. This leads to relatively low semiconductors' conduction losses that contribute the total losses. The DVR often stays in this mode. In boost operation mode (V_{inj}>0), the DVR injects a compensated voltage across the injection transformer when detecting a disturbance in the supply voltage.

When the source voltage V_{source} decreases or increases during under/over voltage condition, the DVR will maintain the desired load voltage magnitude V_{load} constant via injecting a series voltage V_{inj} across the transformer as:

$$V_{inj} = V_{load} + Z_{line} I_{line} - V_{source} \quad (5)$$

where Z_{line} is the line impedance and I_{load} is the load current.

If the voltage source doesn't have any voltage disturbances, then the V_{load} will approximately equal to V_{source} and the DVR will inject a very small amount voltage of (Z_{line} I_{load}) that is needed for compensating the line voltage drop. The load current can be given by:

$$I_{load} = \frac{P_{load} \pm jQ_{load}}{V_{load}} \quad (6)$$

Generally, the DVR is consisting of the following major parts [35, 38].

3.1. Voltage Source Inverter (VSI)

The VSI composes of a storage device and semiconductor power switching devices to convert the DC voltage to AC voltage. It can deliver a sinusoidal output voltage, at the desired magnitude, frequency, and phase angle supplied to distribution lines through an injection transformer. The VSI is used as a temporary replace or generate the supply voltage which is missing. A Sinusoidal Pulse width modulation SPWM inverter using Insulate Gate Bipolar Transistor IGBT switches are utilized in the proposed DVR model. The IGBT is suitable for fast switching and high-efficiency circuits. The PWM is a very efficient technique for producing a sinusoidal output voltage with minimum distortion.

3.2. Boost (Injection) Transformers

In this paper, three single-phase transformers are serially connected with the power distribution lines for the purpose of matching the VSIs with the low voltage levels of these lines. The secondary side of the injection transformer is serially connected to the voltage distribution line, whereas the primary side is attached to the DVR power circuit. The capability of the DVR to supply the required voltage to the secondary distribution network across the series boosting transformer is addressed in [38]. The choice of the injection transformer winding depends on the way it is connected to the load, either connected directly to the load or across a step-down transformer that feeds the load. For three single-phase DVRs, three single-phase injection transformers could be attached to the distribution lines; connect one single-phase transformer for each single-phase DVR. The transformers not only can decrease the voltage requirement of the inverters but also can provide isolation between these inverters.

3.3. Harmonic Filters

These filters could be mounted either on the transformer secondary side or the DVR side of the injection transformer to filter the unwanted harmonics. The features of the DVR side filters are (i) the voltage components are rated at lower values and (ii) high order harmonics of current are not permitted to pass through the transformer windings. In this paper, these filters are installed on the DVR side. The study [39] dealt with the detail of DVR filter design.

3.4. Energy Storage

It provides the required active power for load voltage compensation during voltage disturbance period. It is also possible to supply the needed power on the DC side of the VSI by supplementary bridge AC/DC converter, supplied from an AC auxiliary supply. A DC battery or supercapacitor might be employed as an energy storage device.

3.5. Control Unit

The control of compensating device is carried out in three steps, detection of voltage variation occurring in the system, comparing it with the reference value and production of gate pulses to the VSI necessary to produce the DVR output voltages which will mitigate the voltage variation. The SPWM control method is applied to inverter switching to produce three phase, 50 Hz sine wave voltages on the load side.

4. CONTROL STRATEGY

The basic job of the DVR controller is detecting the balanced/unbalanced voltage disturbances in the power system starting from computing the correction voltage, generating trigger pulses to the SPWM based inverter, correcting any irregularity in the series injected voltage and stopping the trigger pulses as the fault finishes.

The dq0 transformation or Park's transformation method [40-42] is used to control the DVR. The controller in d-q-0 coordinates has better performance than traditional controllers. The dq0 theory gives information about depth and phase shift of the voltage disturbance at the start and ends time periods. This information is treated as instantaneous space vectors. Firstly, the voltage is converted from abc reference frame into dq0 reference. To simplify the transformation, the components of the zero phase sequence are ignored. Figure 2 demonstrates a flowchart of the feed-forward dq0 transformation for detection the voltage disturbances. The figure shows the control strategy of the proposed system.

The controlled variables in the d-q-0 coordinates are then inversely converted to the original voltages that produced the reference voltages to the DVR. The detection process has been executed in all three phases. The proposed control scheme of DVR system depends on the comparison between the reference voltages and actual voltages to generate an error signal. The error signal is utilized as a modulation signal that permits the generation of the SPWM switch pattern for the IGBT power switches that constitute the VSI, to control the resulting voltages.

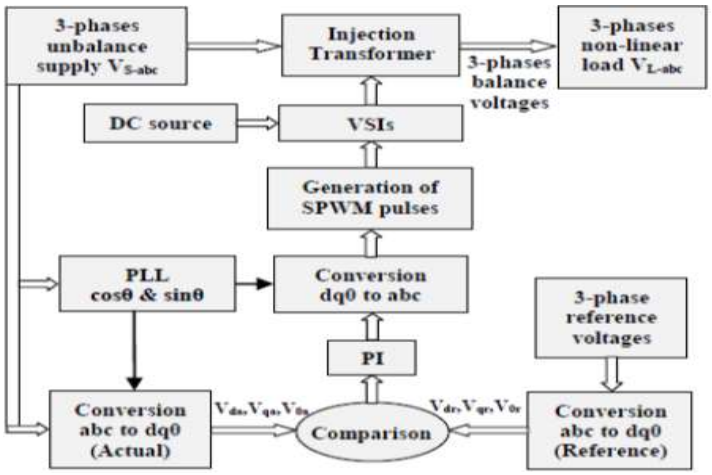

Figure 2. DVR flowchart based on dq0 transformation with a feed-forward control strategy

A Phase-locked Loop PLL circuit [43] is employed to generate a sine wave unit in phase with mains power supply voltage. It maintains a synchronous output signal with a reference input signal in phase and frequency. A PI controller [44] is used to calculate the error value as the difference between the reference value and measured process variable, and reduce the error in outputs by the adjustment of process control inputs.

The control scheme of the DVR shown in Figure 2 is divided into two parts a) Reference signal b) gate signals generated via the SPWM controller. In this scheme, source voltage V_{S-abc} is sensed and is presented as an input to the abc/dq0 transformation block. The same voltage is offered as an input to the PLL block which provides the information of sinθ and cosθ. This will be given as an input to the abc/dq0 block. With these two inputs, this transformation block provides information of actual voltages V_{da}, V_{qa}, and V_{0a}. This information is compared with the corresponding reference parameters V_{dr}, V_{qr} and V_{0r}, when both the quadrature voltage V_{qr} and zero voltage V_{0r} are equal to 0 p.u while the direct voltage V_{dr} equal to 1 p.u. The error is produced and provided as an input to the PI controller. The output signals of the PI controller as well as PLL information is again given as inputs to the dq0/abc block. This block will give pulse information as an input to the SPWM generator to generate gate pulses for the DVR inverter.

Equation (3) determines the transformation process of the three-phase system abc into dq0 stationary frame. In the process, the phase an aligns to the d-axis and orthogonal with the q-axis. θ is known as the angle between the phase a and the d-axis [40].

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (7)$$

The proposed controller will be implemented through simulation using MATLAB/SIMULINK to investigate its efficiency in mitigation of voltage disturbance.

5. SYSTEM IMPLEMENTATION

A simulation circuit diagram of the proposed DVR design shown in Figure 3 is implemented using MATLAB/SIMULINK to mitigate various voltage disturbances.

The system contains three voltage supply blocks, each one is named "*programmable 1-ph voltage source*", to generate three single-phase AC supplies, shifted by 120^{o}, along with the voltage disturbance in the system if any. Each supply has a peak amplitude of $230\sqrt{2}$ V per phase. It is connected or disconnected from the system using a switch which is initially closed and opened to disconnect the main supply whenever a voltage variation is to be created.

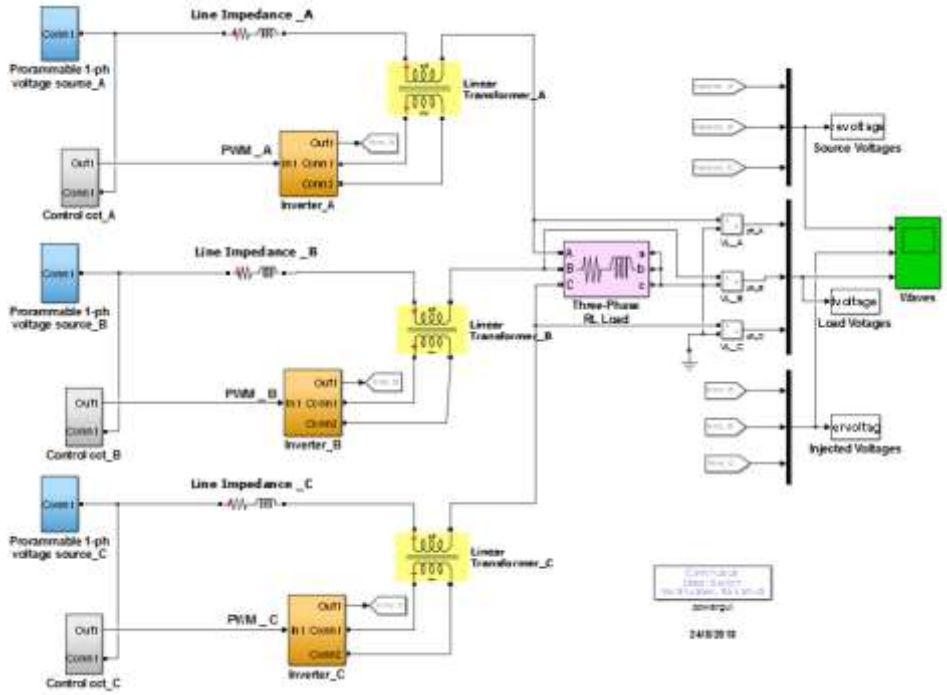

Figure 3. Matlab schematic diagram of dq0 control DVR implementation

In this paper, the model simulation is carried out for two patterns of time periods. In the first one, the faults happen for the three-phase voltages at the same time; the switch opens at 0.04s when the fault is created and closes again at 0.12s to resume normal supply. Another pattern is generated when the phases are disturbed for different time periods; phase A fault occurs for a time period of (0.08-0.12sec), phase B fault for (0.06-0.14sec) and phase C fault for (0.04-0.16sec). For the two proposed time patterns, different types of voltage disturbances, unbalanced and balanced, are applied for each of the three phases.

The supply blocks are followed by three single-phase series RLC impedances, each one named "*Line Impedance*" having a resistance of 1Ω and inductance of 1mH to represent a transmission line. The three transmission lines are connected to three phases star connected inductive load across three single-phase transformers, each one named "*Linear Transformer*". The load impedance referred to as "*Three-Phase RL Load*", rated with 230V, 1kVA at a power factor of 0.92 and has a resistance of 100Ω and inductance of 1mH. The transformers are feeding required compensation voltages to the three lines across three DVRs. Each transformer is rated at 20 kVA and has a turn's ratio of 1:1.

The DVR uses a separate H-bridge cell for each phase labeled as "*Inverter*". The input DC supply to each H-bridge is E=230$\sqrt{2}$ V. Each H-bridge is capable of providing three voltage levels at its output side, E, -E and 0. The "*Control cct*" blocks are utilized to generate the 'PWM' signals that fed the inverter IGBTs' gates. The control schemes used for controlling the outputs of the inverters utilize the dq0 theory. The required DVR voltage is obtained and then processed through a low pass RLC filter of R=10^{-4}Ω, L=0.1mH, C=2.7μF, built in the Inverter block, in order to remove the harmonics.

All the required signals like the three-phase source voltages V_{source}, injected voltages V_{inj}, and load voltages V_L could be read through the "*Waves*" scope.

6. SIMULATED RESULTS

The low voltage distribution system configuration combined with the DVR shown in Figure 3 is simulated using Mathworks Matlab/Simulink and carried out to study the effectiveness and responsiveness of the proposed DVR control strategy under different supply voltage disturbances. The required simulation power distribution system parameters and other constant values are listed in Table 1. The effectiveness of the program will be tested in its fast response and ability to maintaining load voltage constant at rms magnitude of 230V during the voltage disturbance conditions.

Table 1. System parameters

Quality	Symbols	Parameter
source voltage, phase, frequency	V_s, Φ, f	230V, 3-Φ, 50Hz
load power and power factor	S_{load}, P_f	1kVA, 0.92
line impedance	R_l, L_l	1Ω, 1mH
load impedance	R_L, L_L	100Ω, 1mH
DC source voltage	V_{dc}	$230\sqrt{2}$ V
Inverter	VSI	IGBT, 3-arms, 6-pulses
sampling frequency	f_s	2kHz
Injection transformer	N_2/N_1, V_2/V_1	1:1, 230/230V
filter components	R_s, L_s, C_s	10^{-4}Ω, 0.1mH, 2.7μF
PI controller	K_p, K_i	42, 38

The simulation test results for both unbalanced and balanced cases of voltage disturbances were as follows:

6.1. When Voltage Disturbances of the Three Phases Occur During the Same Time Periods

6.1.1. Voltage unbalance disturbance

For unbalance conditions, the DVR device injects suitable unbalanced three-phase voltages, positive or negative based on whether the fault condition is UVU (sag) or OVU (swell).

Cases of the UVU faults in single, two or three phase voltages have been simulated and their results are demonstrated in Figures 4-6, respectively.

Figure 4 shows that a single-phase to ground UVU fault on phase A is created at time t = 0.04s for a duration of 0.08s. During this period, the phase A voltage sags to 125V, i.e. decreases by about 45.6% of its nominal value, 230V (healthy case), causing a percentage of voltage unbalance factor VUF of 17.95%. Other phases are kept constant at 230 V rms. Figure 5 shows voltage sag in two phases A and B to 125V and 170V; this means a reduction by ratios of 45.6% and 26.1%, respectively with VUF of 17.38%, initiated at 0.04s and remain constant until 0.12s with total voltage sag duration of 0.08s. Figure 6 shows that all phase voltages are falling down from their nominal value to 125V, 170V, and 215V; by about 45.6%, 26.1%, and 6.5%, respectively with VUF of 15.28 % during sag time of 0.08s.

The Figures 4-6 also show the voltages that should be injected V_{inj} by the DVR, as well as the compensated load voltage V_L for all the aforementioned failures, respectively. It is seen from the results, the rms load voltage is kept constant at 230V, throughout the simulation, process including the UVU period. Observing that during normal operation, the DVR do nothing, while it is quickly injecting necessary voltage components in order to smooth the load voltage upon detecting voltage sag.

Similarly, the DVR performance under the OVU fault condition could be investigated. Here, the supply voltage swell can be created as illustrated in Figures 7-9 for single, two or three phases, respectively. In Figure 7, the supply rms voltage amplitude of phase A is increased from 230V to 328V, by about 42.6% of nominal voltage with VUF of 12.44%, starting from t=0.04s to 0.12s. The figure also shows the injected voltage that is produced by the DVR in order to correct the load voltage. Also, two single-phase to ground OVU faults of different severity on phases A and B are applied at a time t = 0.04s for a fault duration of 0.08s. In this case, the voltages of phases A and B are disturbed with swells to reach 286V and 328 at rates of 24.3% and 42.6%, respectively causing VUF of 10.1% as shown in Figure 8. Figure 9 shows the voltage swell in all three phases to 244V, 286V, and 328V, which means an increase by rates of 6.1%, 24.3%, and 42.6%, respectively with a VUF of 8.48%.

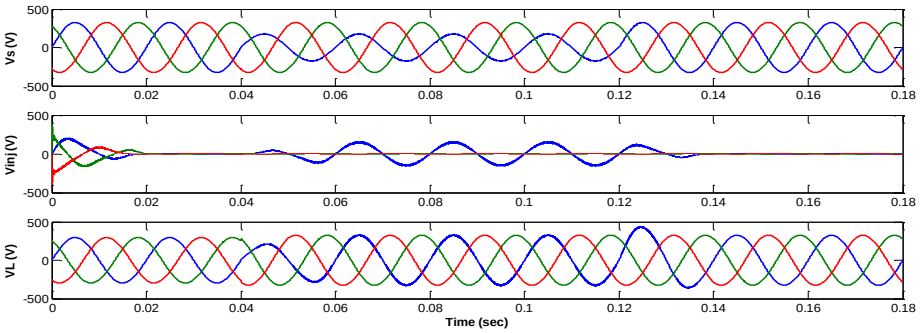

Figure 4. 1-ph UVU; V_A=125V,V_B=V_C=230V; VUF=17.95%

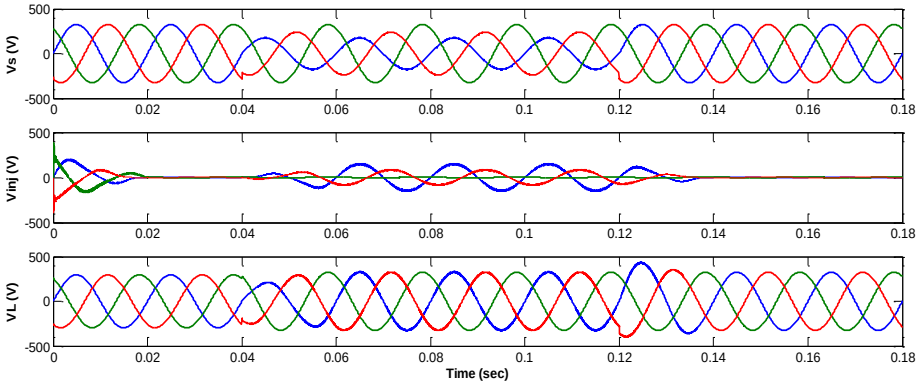

Figure 5. 2-ph UVU; V_A=125V,V_B=170V,V_C=230V; VUF=17.38%

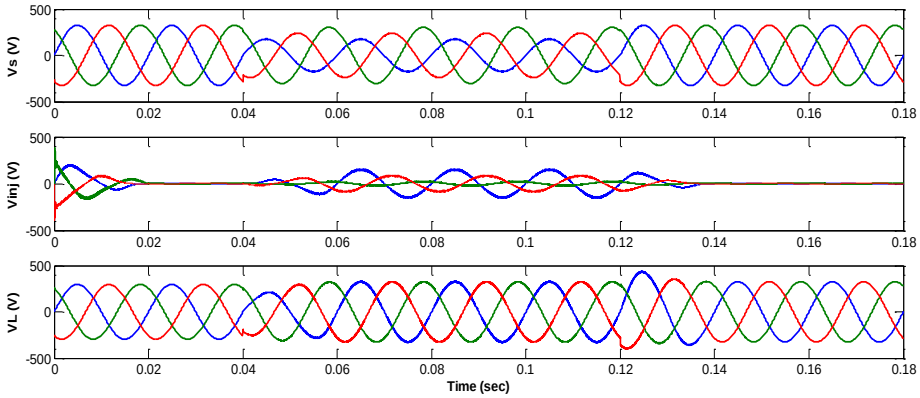

Figure 6. 3-ph UVU; V_A=125V,V_B=170V,V_C=215V; VUF=15.28%

The Figures 7-9 also show how the DVR efficiently compensates the OVU disturbances. The load voltage with the help of the DVR has improved, balanced and remain balanced in the three phases at the nominal value. In the same way of the UVU disturbance case, the DVR activates rapidly to inject a suitable negative voltage to the high distribution lines. Stability and balance can be observed in the load voltage at constant rms value throughout the simulation period, including the unbalance voltage swell event period.

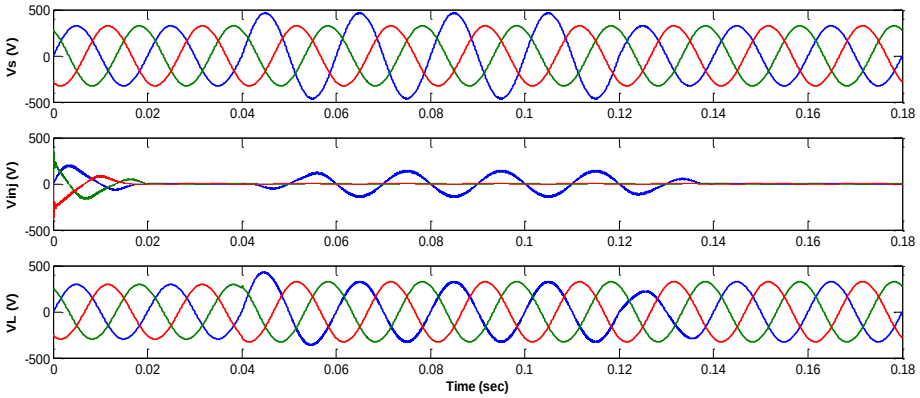

Figure 7. 1-ph OVU; V_A=328V,V_B=V_C=230V; VUF=12.44%

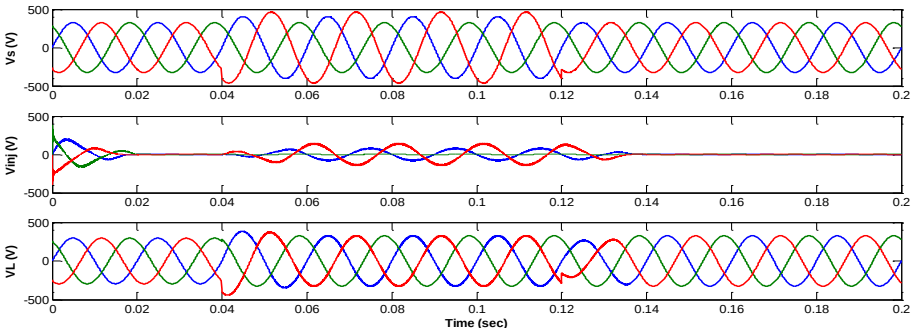

Figure 8. 2-ph OVU; V_A=286V,V_B=328V,V_C=230V; VUF=10.1%

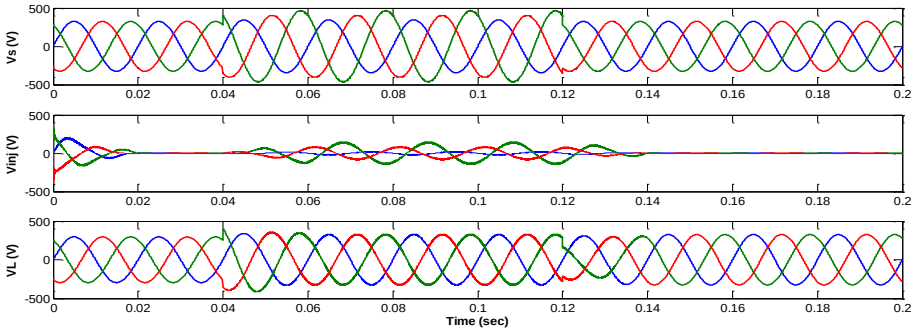

Figure 9. 3-ph OVU; V_A=244V,V_B=286V,V_C=328V; VUF=8.48%

In most cases, the UVU and OVU disturbances occur together as shown in Figure 10, e.g. when phase A drops by 50% from 230V to 115V and phase C rises by 42.6% from 230V to 328V, while phase B remains constant, causing a VUF of 27.44%. The figure also shows how the DVR efficiently compensating this type of faults.

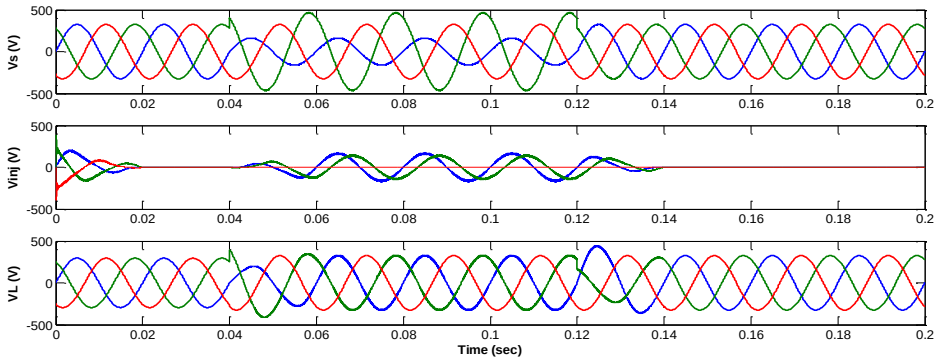

Figure 10. UVU/OVU; V_A=115V,V_B=230V,V_C=328V; VUF=27.44%

6.1.2. Voltage balance disturbance

This means that all the phases are exposed to the same faults during the same time period as shown in Figures 11-13. In the case of undervoltage balance UVB disturbance (or voltage sag), which is a requirement for a temporary decrease in the supply voltage; the DVRs inject equal positive voltage components in all three phases. These components should become in phase with the supply voltages to correct them. The condition of voltage sag could be simulated by producing a balanced three-phase to ground fault at a time t = 0.04s for a duration of 0.08s.

For the system without the DVR, the source voltage in Figure 11 drops by 50% from its nominal value; 230V to 115V with VUF of 0%. The system with the DVR connected, the load voltage swells from 115V to 230V. The same thing will happen when the power system is exposing to an overvoltage balance OVB disturbance (voltage swell) shown in Figure 12, as the voltage in all phases is raised from 230V to 328V with VUF of 0 %. Thus, the inverter voltage will inject a negative rms voltage of 98V to compensate the line voltages to be balanced on 230V.

Sometimes, the system line voltages drop to zero voltage due to the temporary interruptions which may happen in the distribution network. The DVR, in this case, will efficiently compensate the distribution network with the required nominal voltages as investigated in Figure 13. It can be noted from the simulation results of Figures 11-13 that the DVR offers a better capability of voltage sag/swell compensation in terms of the voltage magnitudes.

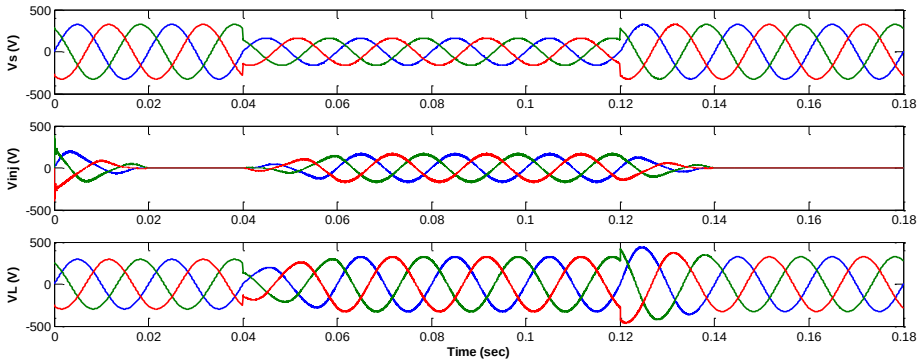

Figure 11. Sag; $V_A=V_B=V_C=115V$; VUF=0%

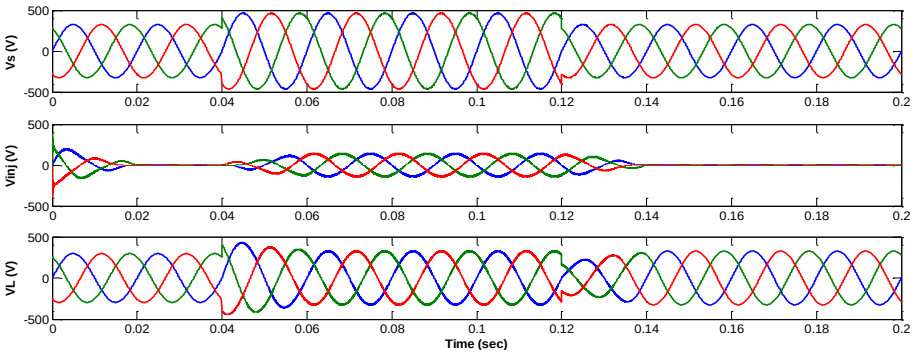

Figure 12. Swell; $V_A=V_B=V_C=328V$; VUF=0%

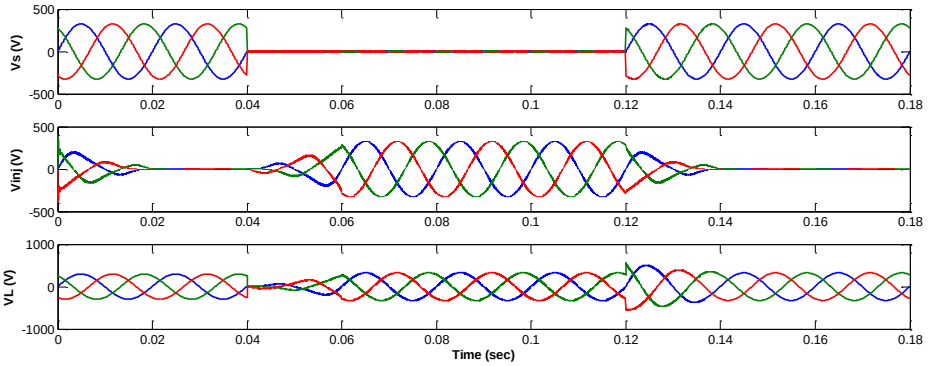

Figure 13. Zero balanced fault; $V_A=V_B=V_C=0V$; VUF=∞

6.2. When voltage disturbances of the three phases occur during different time periods

When the phases A, B, and C are exposing to different voltage faults during different time periods, such as zero voltage fault for phase A during a period of (0.08-0.12sec), UVU (or sag) disturbance of 115V in phase B through a period of (0.06-0.14sec), and OVU (or swell) disturbance of 328V in phase C within a period of (0.04-0.16sec) shown in Figure 14. In this case, the values of the VUF will vary through the three time periods as follows 14.06%, 27.82%, and 65.1%, respectively. The figure shows how the DVR able to efficiently compensate the three phases when exposing to different faults for different time periods.

It can be concluded from all the previous findings, the DVR is capable of producing the wanted voltage components for the three phases for any type of voltage balance/unbalance disturbance rapidly for a time not exceed one cycle and help to keep a balanced and constant load voltage at the nominal value.

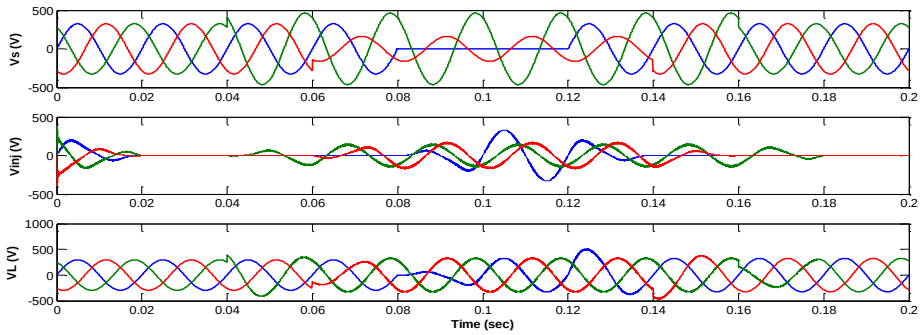

Figure 14. UVU/OVU; V_A=0V,V_B=115V,V_C=328V at different values of time periods and VUF

7. CONCLUSIONS

This paper describes the problem of under/over and unbalanced/balanced voltage disturbances constantly occurring on the low voltage distribution system in Iraq country and how to solve this problem using the DVR device. Although an open-loop feed-forward method was used to control the DVR, the simulation results showed clearly that the DVR can mitigate efficiently and reliably the unbalanced/balanced voltage disturbances for various combinations. The DVR can handle all disturbance situations without any difficulties and injects the appropriate voltage component to correct promptly any irregularity in the supply voltage in order to maintain the load voltage balanced and constant at the nominal value. The proposed control method is found to be very effective, highly accurate, simple, and fast-dynamic response for identifying and clearing any voltage unbalance/balance disturbance that may occur in the low voltage distribution systems.

REFERENCES

[1] E.F.M. Masoum, Power Quality in Power Systems and Electrical Machines, 2nd Ed, *Academic Press*, 2015.
[2] B. Singh, A. Chandra, K. Al-Haddad, Power Quality: Problems and Mitigation Techniques, *1st Ed, John Wiley & Sons Ltd*, 2015.
[3] S. Khan, B. Singh, P. Makhija, "A review on power quality problems and its improvement techniques," 2017 *Innovations in Power and Advanced Computing Technologies (i-PACT)*, 21 – 22 April 2017.
[4] C. Bayliss, B. Hardy, Transmission and Distribution Electrical Engineering, *4th Ed. Newnes/Elsevier, Inc.* 2011.
[5] R.C. Dugan, M.F. McGranaghan, S. Santoso, H.W. Beaty, Electrical power systems quality, *2nd Ed. New York: McGraw Hill*, 2003.
[6] G. Gupta, W. Fritz, "Voltage Unbalance for Power Systems and Mitigation Techniques a Survey," *IEEE 1st Inter. Conf. on Power Electronics. Intelligent Control and Energy Systems (ICPEICES)*, 4-6 July 2016.
[7] A.H. Abed, J. Rahebi, H. Sajir, A. Farzamnia, "Protection of sensitive loads from voltages fluctuations in Iraqi grids by DVR," *IEEE 2nd Inter. Conf. on Automatic Control and Intelligent Systems (I2CACIS)*, 21-21 Oct 2017.
[8] M.W. Siti, D.V. Nicolae, A.A. Jimoh, A. Ukil, "Reconfiguration and Load Balancing in the LV and MV Distribution Networks for Optimal Performance," *IEEE Trans. on Power Delivery*, vol. 22, no. 4, pp. 2534-2540, 2007.
[9] T.H. Chen, J.T. Cherng, "Optimal phase arrangement of distribution transformers connected to a primary feeder for system unbalance improvement and loss reduction using genetic algorithm," *IEEE Trans. on Power Systems*, vol. 15, no. 3, pp. 994-1000, 2000.

[10] IEEE 1547.2-2008- IEEE Application Guide for IEEE Std 1547(TM), *IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*.
[11] H.D. de Macedo Braz, B.A. de Souza, "Distribution Network Reconfiguration Using Genetic Algorithms with Sequential Encoding: Subtractive and Additive Approaches," *IEEE Trans. on Power Systems*, vol. 26, no. 2, pp. 582-593, 2011.
[12] S. Jazebi, M.M. Hadji, R.A. Naghizadeh, "Distribution Network Reconfiguration in the Presence of Harmonic Loads: Optimization Techniques and Analysis," *IEEE Trans. on Smart Grid*, vol. 5, no. 4, pp. 1929-1937, 2014.
[13] Q. Peng, Y. Tang, S.H. Low, "Feeder Reconfiguration in Distribution Networks Based on Convex Relaxation of OPF, *IEEE Trans. on Power Systems*, vol. 30, no. 4, pp. 1793-1804, 2015.
[14] P.K. Dhal, C.C.A. Rajan, "Power quality improvement based on uninterruptible power supply (UPS) in distribution system," *2nd Inter. Conf. on Electronics and Communication Systems (ICECS)*, 26-27 Feb 2015.
[15] A.H.K. Asadi, H.M. Naimi, A. Jahangiri, "A new controlled superconducting magnetic energy storage for dynamic stabilization of distributed generation in islanding mode of operation," *Inter. Trans. on Electrical Energy Systems*, vol. 27, no. 11, 2017.
[16] J.D. Kueck, D.T. Rizy, "Voltage and current unbalance compensation using a static var compensator," *IET Power Electronics*, vol. 3, no. 6, pp. 977-988, 2010.
[17] McCarrel, Bahry, Folkesson, Berube, "Distribution Series Capacitor Application for Improved Motor Start and Flicker Mitigation," *IEEE/PES Transmission and Distribution Conf. and Exhibition*, 21-24 May 2006.
[18] S.H. Hosseini, A. Nazarloo, "Voltage unbalance reduction by distribution static compensator in a case study network," *7th Inter. Conf. on Electrical and Electronics Engineering (ELECO)*, 1-4 Dec 2011.
[19] K. Gaeid, M. Hamood, "Unified Power Quality Conditioner Model Based with Series and Shunt Filters," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 7, no. 3, pp. 742-756, 2016.
[20] M.T.L. Gayatri, A.M. Parimi, A.V.P. Kumar, "Application of Dynamic Voltage Restorer in microgrid for voltage sag/swell mitigation, *IEEE Power, Communication and Information Technology Conf. (PCITC)*, 15-17 Oct 2015.
[21] T. AppalaNaidu, "The Role Of Dynamic Voltage Restorer (DVR) in improving power quality," *2nd Inter. Conf. on Advances in Electrical, Electronics, Information, Communication, and Bio-Informatics (AEEICB)*, 27-28 Feb 2016.
[22] V. Dargahi, A.K. Sadigh, K. Corzine, "Medium voltage dynamic voltage restorer (DVR) based on DFCM converter for power quality improvement," *Clemson University Power Systems Conference (PSC)*, 8-11 March 2016.
[23] S.R. Reddy, P.V. Prasad, G.N. Srinivas, "Performance comparison of DVR by various compensation methods, *6th IEEE Power India International Conference (PIICON)*, 5-7 Dec 2014.
[24] T.S. Saggu, L. Singh, "Comparative analysis of custom power devices for power quality improvement in non-linear loads," *2nd Inter Conf. on Recent Advances in Engineering & Computational Sciences (RAECS)*, 21-22 Dec 2015.
[25] J. Praveen, B.P. Muni, S. Venkateshwarlu, H.V. Makthal, "Review of dynamic voltage restorer for power quality Improvement," *30th Annual Conf. of IEEE Industrial Electronics Society IECON*, 2-6 Nov 2004.
[26] E. Babaei, M.F. Kangarlu, "Sabahi M. Mitigation of Voltage Disturbances Using Dynamic Voltage Restorer Based on Direct Converters," *IEEE Trans. on Power Delivery*, vol. 25, no. 4, pp. 2676-2683, 2010.
[27] A.K. Sadigh, K.M. Smedley, "Review of voltage compensation methods in dynamic voltage restorer (DVR)," *IEEE Power and Energy Society General Meeting*, 22-26 July 2012.
[28] K. Bhumkittipich, N. Mithulananthan, "Performance Enhancement of DVR for Mitigating Voltage Sag/Swell using Vector Control Strategy," *Energy Procedia*, vol. 9, pp. 366-379, 2011.
[29] S.V.R.L. Kumari, M.U. Vani, "Dynamic Voltage Restorer for Sag and Swell Issues in Power System," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 11, no. 3, pp. 1243-1250, 2018.
[30] M. Zadehbagheri, R. Ildarabadi, M.B. Nejad, "Review of Dynamic Voltage Restorer Application for Compensation of Voltage Harmonics in Power Systems," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 5, no. 1, pp. 58-71, 2017.
[31] Fu-Zhuan Wu, Su-ping Pei, "The Research and Implementation of Dynamic Voltage Restorer with Power Factor Correction," 3rd Inter. Workshop on Intelligent Systems and Applications, 28-29 May 2011.
[32] N.H. Mohammadi, S.I. Bektas, S.H. Hosseini, E. Babaei, M. Sabahi, "A conventional dynamic voltage restorer with fault current limiting capability," *Procedia Computer Science*, vol. 120, pp. 750-757, 2017.
[33] M. Masihian, E. Farjah, "Modified control technique for improvement of DVR transient response," *First Power Quality Conf.*, 14-15 Sept 2010.
[34] W. Jing, X. Aiqin, S. Yueyue, "A survey on control strategies of dynamic voltage restorer," *13th International Conference on Harmonics and Quality of Power*, 28 Sept - 1 Oct 2008.
[35] A. Zargar, S.M. Barakati, "A new dynamic voltage restorer structure based on three-phase to single-phase AC/AC matrix converter," *20th Conf. on Electrical Power Distribution Networks Conference (EPDC)*, 28- 29 April 2015.
[36] P. Pillay, M. Manyage, "Definitions of voltage unbalance," *IEEE Power Eng. Review*, vol. 21, no. 5, pp. 50-51, 2001.
[37] S. Preetha, R. Bhavani, N.R. Prabha, "Design of ultra-capacitor based DVR for power quality improvement, "*Inter. Conf. on Circuit, Power and Computing Technologies (ICCPCT)*, 18-19 March 2016.
[38] A. Ghosh, G. Ledwich, "Structures and control of a dynamic voltage regulator (DVR)," *IEEE Power Engineering Society Winter Meeting, Conference Proceedings*, 28 Jan - 1 Feb 2001.
[39] S.J. Yao, Z.G. Zhu, H.Y. Zhang, J.W. Cao, G.Y. Zhang, "The Design of Filter Parameters of Dynamic Voltage Restorer in Medium Voltage Network," *Applied Mechanics and Materials*, vol. 654, pp. 133-141, 2014.
[40] M.F. Schonardie, D.C. Martins, "Application of the dq0 transformation in the three-phase grid-connected PV systems with active and reactive power control," *IEEE Inter. Conf. on Sustainable Energy Tech.*, 24-27 Nov 2008.

[41] M. Faisal, Md.S. Alam, Md.I.M. Arafat, Md.M. Rahman, Sk.Md.G. Mostafa, "PI controller and park's transformation based control of dynamic voltage restorer for voltage sag minimization," *9th Inter. Forum on Strategic Technology (IFOST)*, 21-23 Oct 2014.
[42] D.N. Katole, M.B. Daigavane, S.P. Gawande, P.M. Daigavane, "Analysis, Design and Implementation of Single Phase SRF Controller for Dynamic Voltage Restorer under Distorted Supply Condition," *Energy Procedia*, vol. 117, pp. 716-723, 2017.
[43] D. Xie, D. Zhang, P. Gao, "Research on phase-locked loop control and its application," *IEEE Information Technology, Networking, Electronic and Automation Control Conf.*, 20-22 May 2016.
[44] M.T. Ali, F. Abbas, A. Nadeem, M. Yaqoob, S.M. Malik, M.J. Iqbal, "Effect of PI controller on efficiency of dynamic voltage restorer for compensation of voltage quality problems," *16th Inter. Power Electronics and Motion Control Conf. and Exposition*, 21-24 Sept 2014.

BIOGRAPHIES OF AUTHORS

Jamal A.K. Mohammed was born in Iraq, in 1967. He obtained his B.Sc. of Electrical Engineering degree in 1996 and his M.Sc. of Electrical Engineering degree in 2002 from University of Technology, Baghdad. His Ph.D. degree was awarded in 2007 by University of Technology, Iraq-Baghdad. He is an Assistant Professor at the Department of Electromechanical Engineering, University of Technology. His research interests include electrical machines, electrical drives, power electronics, Elevators, and renewable energy (solar). He has published close to 30 papers and has supervised several M.Sc. and Ph.D. thesis.

Arkan Ahmed Hussein received his PhD in Electrical Engineering from the Department of Electrical Engineering, Jamia Millia Islamia, New Delhi, India, in 2015. He obtained his BSc and MSc in Electrical Engineering from the University of Technology, Iraq, in 1998 and 2005, respectively. Currently, he is an Assistant Professor in the Tikrit University, Iraq. His research interests include power system operation and control, automatic generation control, soft computing techniques in power systems and HVDC transmission systems.

Sahar R.AL-Sakini was born in Iraq, in 1965. she obtained her B.Sc. in Electrical Engineering in 1987 and her M.Sc. in 1999 from University of Technology, Baghdad. Her Ph.D. degree was awarded in 2003 by University of Technology, Baghdad-Iraq. Currently she is a lecturer at the Department of Electromechanical Engineering, University of Technology. She published many research in power system and renewable energy.